Polyphase CIC Filter Structures for Digital Receivers

R.Latha , Dr.P.T.Vanathi

Abstract-There are multiple ways to implement a decimator filter. In this paper, first approach addresses usage of Cascaded Integrator Comb (CIC) filter transfer function through the polynomial formula with zeros and poles. Second approach is to implement a conventional poly-phase comb filter and the third approach is based on modified poly-phase comb filter. A Power efficient poly-phase decomposition comb filter with a clock distribution algorithm for its memory elements is presented. The proposed algorithm results in a significant reduction in the dynamic power consumption, comparing with the conventional poly-phase decomposition comb filter that is widely used as a first stage of decimation process in sample rate conversion for multi-rate telecommunication receivers. A general form of the proposed clock distribution algorithm is presented with respect to the decimation factor of the poly-phase comb filter. It is shown that, using the proposed clock distribution algorithm reduces the dynamic power consumption of the memory elements for a second order poly-phase comb filter when compared with polynomial CIC filter. As well as, we can reduce the dynamic power consumption of the memory elements for a third order poly-phase comb filter. It is estimated such that power consumed in modified poly-phase comb decimation filter is less than the power consumed in conventional poly-phase comb decimation filter.

Index Terms– Polynomial, CIC,Comb filter, Low power, Clock Distribution, Poly-phase Decomposition, Decimation filter.

1 INTRODUCTION

Decimation filter has wide application in both the analog and digital system for data rate conversion as well as filtering [1]. The decimating low-pass filter accepts input samples from the mixer output at the full Analog to Digital (A/D) sampling frequency f_s. It utilizes digital signal processing to implement a Finite Impulse Response (FIR) filter transfer function [2]. The filter passes all signals from 0 Hz up to a programmable cutoff frequency or bandwidth, and rejects all signals above that cutoff frequency. This digital filter is a complex filter, which processes both I and Q signals from the mixer. At the output, one can select either I and Q (complex) values or just real values, depending on your system requirements. In multi-rate receivers, decimation filters are required to perform channel select filtering and Sample Rate Conversion (SRC) to the base-band of the selected channel. Reducing the power consumption of the decimation filter is considered as one of the most important goals, since it operates at a high sampling frequency. That is why multiplier free Cascaded Integrator Comb Filter (CIC) is widely used in multi-rate receiver designs [3] . However, since the integrator part of the CIC decimation filter still works at the higher input sampling frequency, its power consumption is still high. Recently, lower power consumption has been achieved using the FIR filter and the Poly-FIR filter.

2 POLYNOMIAL CIC FILTER

Fig.1 shows the block diagram of the polynomial CIC filter. The output for each time sample is determined by the current input, previous input, and previous output. In order to realize this design, registers are used to store the previous input sample and output sample. Fig.2 shows the digital circuit to implement the polynomial CIC filter. Each of the multiplication is implemented using a CSD multiplier where each multiplier is implemented using shift register and adder.

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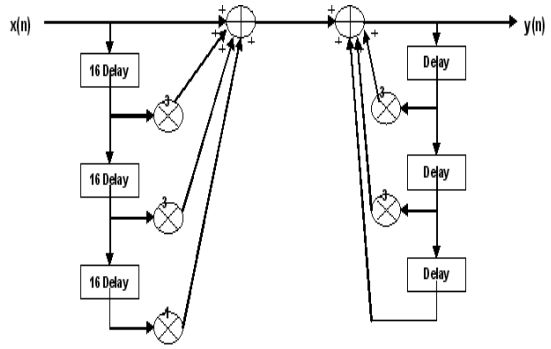

Fig. 1 Block Diagram of Polynomial CIC Filter

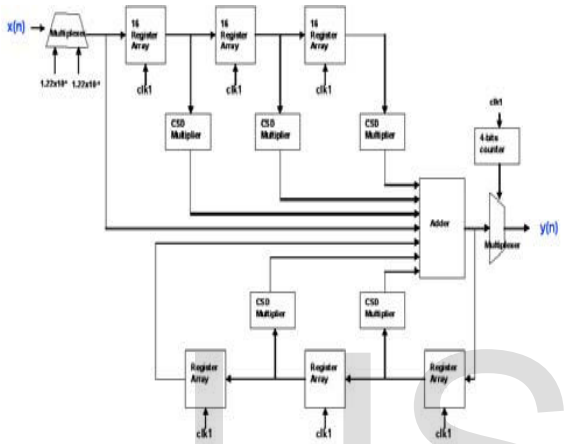

Fig. 2 CIC Filter Implementation using Polynomial Expansion

3 CONVENTIONAL POLYPHASE FILTER

The poly-phase structure of comb decimation filter with a decimation factor *M*, is presented as shown in Fig.3. Several researches used that polyphase comb filter as a first stage of their modified decimation filters. The reason for using that polyphase comb filter is because its sub-filters, $E_m(z)$, are operating at a lower sampling rate (f_s /M), where f_s is the output sampling frequency of Sigma Delta (Σ-Δ) A/D Modulator. Consequently the power consumption of the poly-phase comb filter and the successive decimation filters is reduced [4]. From Fig.3 following important notes are observed:

I. There is another group of memory elements before the decimation process, acting as input registers, still working at the input sampling frequency, shown by dashed area in Fig.3 and it decimates by M.

II. The ratio of those input registers to the total number of registers equals 1/k. Subsequently, their power consumption cannot be neglected for low filter orders.

III. Not all of the input registers have to work at the input sampling frequency. Instead, they should extract the right data only at every f_s /M.

Based on the previous notes, in this work a novel clock distribution algorithm is presented for the input registers of the polyphase comb decimation filter, illustrated in Fig.4, such that their operating frequencies are a multiple division of the higher input sampling rate, f_s [5]. Consequently, their power consumption is reduced .

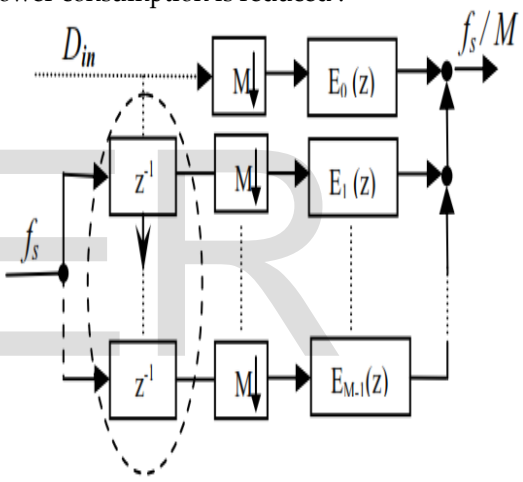

Fig. 3 Poly-phase Decomposition of Comb Decimation Filter

Fig. 4 (a) – (c) show the block diagram of conventional poly-phase Comb decimation filter for decimation factors of 2, 4, and 8.The proposed clock distribution algorithm is applied on second and third order polyphase decimation filters with different decimation factors, since they are widely used in SRC for their low complexity and low Pass-band droop [6]. The dynamic power reduction ratio is then estimated for the memory elements of those modified polyphase comb decimation filters,with respect to the conventional poly-phase comb filter[7].

4 MODIFIED POLYPHASE FILTER

The corresponding block diagrams of the modified comb filter is illustrated in Fig. 5 (*a*), (*b*), and (*c*), for different decimation factors 2, 4, and 8, respectively. The proposed clock distribution algorithm for the input registers of the polyphase comb decimation filter is based on reducing the useless switching activities of the input registers, as result of their high operating frequency, f_s [8]. The proposed clock distribution algorithm is applied on the second and third order poly phase comb decimation filter with different decimation factors, 2, 4 and 8.

Studying Fig 4 and Fig 5, carefully, one can notice that, not all of the input registers of the data input distribution and clock distribution are proposed for those input registers [9].

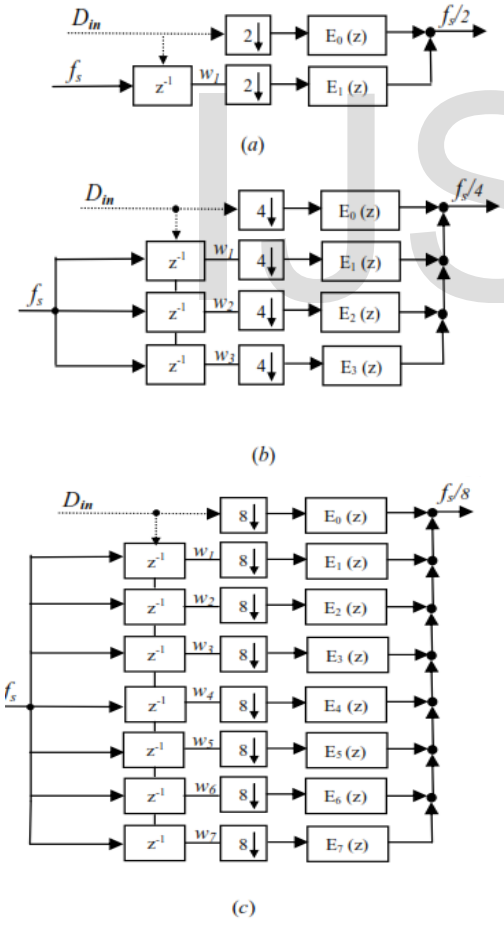

Fig. 4(a) – (c) Block Diagram of Conventional Poly-phase Comb Decimation Filter for Decimation Factors of 2, 4, and 8.

The modified poly-phase CIC decimation filter shows considerable reduction in their dynamic power consumption, since the average power consumption of any digital signal processing system is proportional to the operating frequency [10].

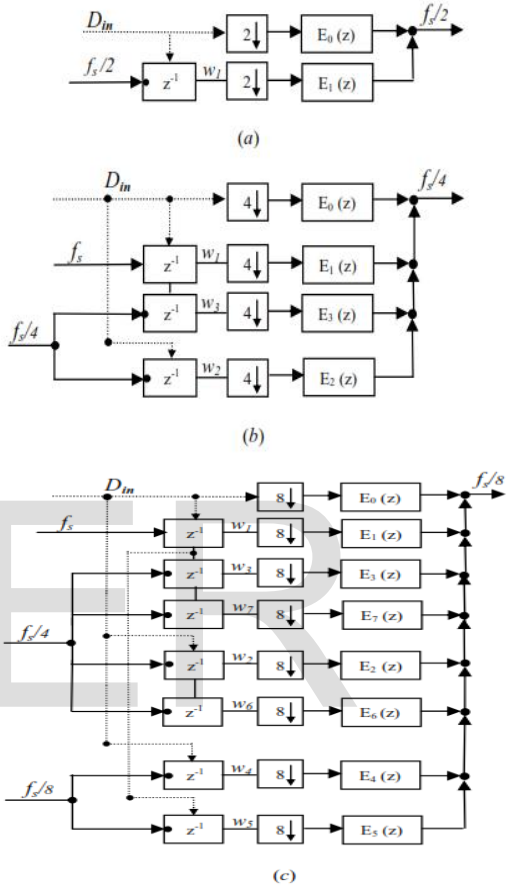

Fig.5 Block Diagram of the Modified Poly-phase Comb Decimation Filter for Decimation Factors 2, 4, and 8.

5 SIMULATION RESULTS

First a VHDL code is written for polynomial CIC filter and it is compared with poly-phase filter. Then a VHDL code is written for both conventional and modified CIC decimation filters and tested on a Field Programmable Gate Array (FPGA) chip. Both second and third order conventional and modified filters are implemented with different decimation factors 2,4 and 8. The Filters are then simulated using Modelsim software. Fig.6 shows the simulation result of polynomial CIC filter. Figs. 7-10 represent the simulation of

conventional poly-phase and modified poly-phase for the decimation factors of 2 and 4.

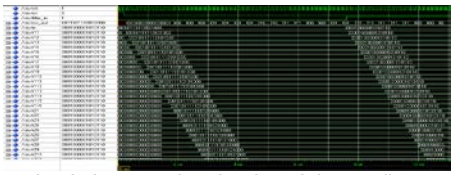

Fig. 6 Simulation Results of Polnomial CIC Filter

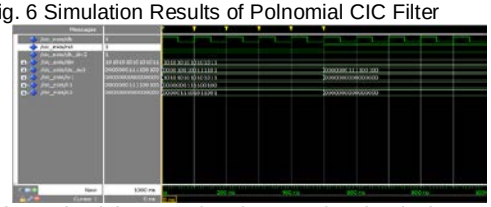

Fig. 7 Simulaion Results of Convenional Polyphase Comb Decimation Filter for M=2

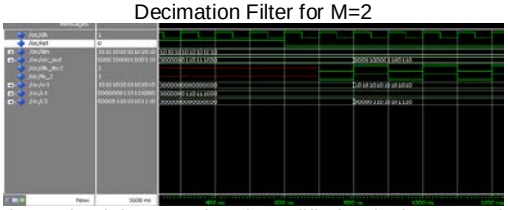

Fig. 8 Simulaion Results of Modified Polyphase Comb Decimation Filter for M=2

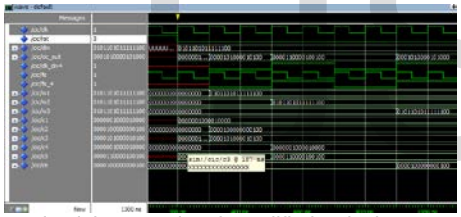

Fig. 10 Simulaion Results of Modified Polyphase Comb Decimation Filter

Studying the simulation results, reducing the operating frequency of some input registers results in reducing the switching activity of them. Consequently their power consumption is reduced. The improvement in power efficiency is clearly indicated in Table 1.

TABLE 1
POWER REDUCTION RATIO

Decimation Factor	Conventional Polyphase Filter	Modified Polyphase Filter	Power Efficiency
M=2	59	58	1.70%
M=4	115	108	6.09%
M=8	122	113	7.48%

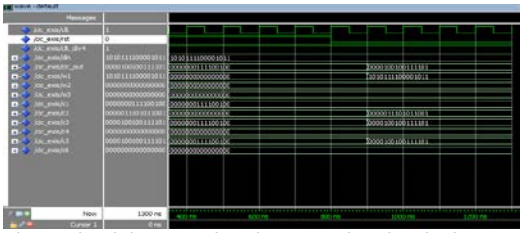

Fig. 9 Simulaion Results of Convenional Polyphase Comb Decimation Filter for M=4

6 CONCLUSION

With the background information, it is proposed to develop a novel clock distribution algorithm for the input register of the poly-phase comb decimation filter. A general form of the new clock distribution algorithm, for a decimation factor M > 2, is developed such that one can simply determines the operating frequencies of the input registers. The new clock distribution algorithm is applied on a third and a second order comb decimation filter for several decimation factors. The new algorithm has significantly reduced the dynamic power consumption upto 7.48% of the memory elements of the poly-phase comb filter for decimation factors 2, 4 and 8 respectively.

REFERENCES

[1] E. B. Hogenauer, "An economical class of digital filters for decimation and interpolation," IEEE Trans.Acoust., Speech, Signal Processing, vol. 29, pp. 155162,April 1981.
[2] Y. Gao, L. Jia, J. Isoaho, and H. Tenhunen, "A comparison design of comb decimators for sigma–delta analog-to-digital converters," Anal. Integr. Circuits Signal Processing, vol. 22, pp. 51–60, Jan. 2000.
[3] Y. Gao, L. Jia, and H. Tenhunen, "Low-power implementation of a fifth order comb decimation filter for multi-standard transceiver application," in Proc. Int.Conf. Signal processing Application Technology,ICSPAT, Oct. 1999.
[4] H. Aboushady, Y. Dumonteix, M. M. Loerat, and H. Mehrezz, "Efficient polyphase decomposition of combdecimation filters in S-Δ analog-to-digital converters," IEEE Trans. on Circuits & Systems-II: Analog and Digital Signal Processing, vol. 48, pp. 898-903, Oct.2001.
[5] G.J. Dolecek , S. K. Mitra, and K. Sanjit, "A New Two-Stage CIC-Based Decimation Filter," 5 IEEE Int. Symp. on Image and Signal Processing and Analysis, Istanbul, Turkey, pp. 218 - 223, Sept. 2007.
[6] Dia, S.M. Thibeault, and C. Gagnon, "A Very High Speed and Efficient CIC Decimation Filter Core,"IEEE North-East Workshop on Circuits and Systems, Gatineau, Que, PP. 61-64, June 2006.
[7] G.J. Dolecek, and S.K. Mitra, "Stepped Triangular CIC-Cosine Decimation Filter," IEEE Sym. on Signal Processing, Rejkjavik, pp. 26 - 29, June 2006.
[8] G.J. Dolecek and J.D. Carmona, "A new Cascaded Modified CIC-Cosine Decimation Filter," ISCAS 2005, Japan, vol. 4, pp. 23-26, May 2005.
[9] S.K. Mitra, "Efficient multistage comb-modified rotted sinc (RS) decimator," Proc. EUSPCO-2004, Austria,pp.1425-1427, Sept. 2004.
[10] Shailesh B. Nerurkar, Khalid H. Abed, Raymond E. Siferd and Vivek Venugopal (2002) , 'Low Power Sigma Delta Decimation Filter', IEEE 45th Midwest Symposium on Circuits and Systems, MWSCAS-2002, Vol.1 ,pp. 647-650.

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